



MITS

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE
(Deemed to be University under section 3 of UGC Act, 1956)

EXAMINATION SECTION
CIRCULAR
ACADEMIC YEAR: 2026-27

All the M.Tech. II Year I Semester (R25) students are hereby informed that the **Mid Term Test - I** for **Skill Enhancement Course-III** will be conducted as per the time table given below.

TIME TABLE - MID TERM TEST -I
M.Tech - VLSI Design and Embedded Systems

Section	Course Name & Code	Date	Timings	Venue
A	Digital Signal Processor- 25MBVESSC03	16-10-2026	09.30 AM to 11.30 AM	Laxmi Block LAB-103

Date: 15-10-2026

CONTROLLER OF EXAMINATIONS

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Madanapalle Institute of Technology & Science
(Deemed to be University)
MADANAPALLE - 517 325, A. P.

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Note: HoD is requested to circulate among the faculty members concerned